- 1 1. A method comprising:
- 2 monitoring the temperature of a cache memory; and
- in response to a detection of a temperature
- 4 condition, transitioning the cache memory from a write-back
- 5 cache to a write-through cache.
- 1 2. The method of claim 1 including monitoring the
- 2 temperature of a ferroelectric polymer cache memory.
- 1 3. The method of claim 1 including adjusting the
- 2 operation of a system using said memory at a first
- 3 temperature and, in response to the detection of a higher,
- 4 second temperature, transitioning the cache from a write-
- 5 back cache to a write-through cache.
- 1 4. The method of claim 3, including slowing an
- 2 operation of said system at said first temperature.
- 1 5. The method of claim 3 including reducing pre-
- 2 fetching at said first temperature.
- 1 6. The method of claim 3 including adjusting what
- 2 data is cached based on the detection of said first
- 3 temperature.

- 1 7. The method of claim 3 including shutting off the
- 2 said cache memory at a temperature above said second
- 3 temperature.
- 1 8. The method of claim 7 including monitoring for a
- 2 temperature lower than said second temperature.
- 1 9. The method of claim 8 including, upon detecting a
- 2 lower temperature, resuming operation of said cache memory.
- 1 10. The method of claim 8 including waiting for a
- 2 power cycle before resuming cache operations.
- 1 11. The method of claim 7 including shutting off said
- 2 cache memory and invalidating cache lines in said cache
- 3 memory.
- 1 12. The method of claim 1 including flushing a cache
- 2 line in said cache memory that has not been written through
- 3 to a source memory.
- 1 13. An article comprising a medium storing
- 2 instructions that, if executed, enable a processor-based
- 3 system to:
- 4 monitor the temperature of a cache memory; and

- 5 in response to the detection of a temperature
- 6 condition, transition the cache memory from a write-back
- 7 cache to a write-through cache memory.
- 1 14. The article of claim 13 further storing
- 2 instructions that, if executed, enable a processor-based
- 3 system to monitor the temperature of a ferroelectric
- 4 polymer cache memory.
- 1 15. The article of claim 13 further storing
- 2 instructions that, if executed, enable a processor-based
- 3 system to adjust the operation of a system using said
- 4 memory at a first temperature and, in response to the
- 5 detection of a higher, second temperature, transition the
- 6 cache memory from a write-back to a write-through cache.
- 1 16. The article of claim 13 further storing
- 2 instructions that, if executed, enable a processor-based
- 3 system to shut off the said cache memory at a temperature
- 4 above said second temperature.
- 1 17. The article of claim 13 further storing
- 2 instructions that, if executed, enable a processor-based
- 3 system to flush a cache line in said cache memory that has
- 4 not been written through to a source memory.

- 1 18. The article of claim 17 further storing
- 2 instructions that, if executed, enable a processor-based
- 3 system to monitor for a temperature lower than said second
- 4 temperature.
- 1 19. The article of claim 18 further storing
- 2 instructions that, if executed, enable a processor-based
- 3 system to resume operation of said cache memory upon
- 4 detecting a lower temperature.
- 1 20. The article of claim 18 further storing
- 2 instructions that, if executed, enable a processor-based
- 3 system to wait for a power cycle before resuming cache
- 4 operations.
- 1 21. The article of claim 16 further storing
- 2 instructions that, if executed, enable a processor-based
- 3 system to shut off the cache and invalidate all the cache
- 4 lines.
- 1 22. The article of claim 13 further storing
- 2 instructions that, if executed, enable a processor-based
- 3 system to transition the cache memory from a write-back to
- 4 cache to a write-through cache memory at a first, higher
- 5 temperature and to adjust for the slower speed of the cache

- 6 memory at a second temperature lower than said first
- 7 temperature.
- 1 23. The article of claim 22 further storing
- 2 instructions that, if executed, enable a processor-based
- 3 system to reduce the speed of operations at said second
- 4 temperature.
- 1 24. The article of claim 22 further storing
- 2 instructions that, if executed, enable a processor-based
- 3 system to reduce pre-fetching at said second temperature.
- 1 25. The article of claim 22 further storing
- 2 instructions that, if executed, enable a processor-based
- 3 system to adjust the caching of data based on the detection
- 4 of said second temperature.
- 1 26. A processor-based system comprising:
- a processor;
- a disk drive coupled to said processor;
- a cache memory coupled said processor; and
- a storage to store a cache driver to monitor the
- 6 temperature of said cache memory and in response to the
- 7 detection of a temperature condition, transition the cache
- 8 memory from a write-back cache memory to a write-through
- 9 cache memory.

- 1 27. The system of claim 26 wherein said cache memory
- 2 is a ferroelectric polymer cache memory.
- 1 28. The system of claim 26 wherein said cache memory
- 2 is a flash memory.
- 1 29. The system of claim 26 wherein said storage
- 2 stores instructions that enable dirty lines to be flushed.
- 1 30. The system of claim 26 wherein said storage
- 2 stores instructions that enable the system to adjust for
- 3 reduced speed operation at a first temperature, switch to a
- 4 write-through cache memory at a second higher temperature,
- 5 and invalidate cache lines and shut off the cache memory at
- 6 still a higher temperature.
- 1 31. The system of claim 30, said storage further
- 2 storing instructions that enable the cache memory to return
- 3 to full speed operation.
- 1 32. The system of claim 30 wherein said storage
- 2 stores instructions that enable the system to wait for
- 3 reduced speed temperature range to resume cache operations
- 4 after shutting off the cache memory in response to a
- 5 temperature condition.

- 1 33. The system of claim 30 wherein said storage
- 2 stores instructions that enable the system to resume cache
- 3 operations after shutting off the cache memory in response
- 4 to a cache condition by initially resuming reduced speed
- 5 operations in a first stage and thereafter resuming normal
- 6 operations.
- 1 34. The system of claim 26 wherein said cache memory
- 2 includes a temperature sensor.
- 1 35. A circuit comprising:
- a component to receive an indication of the
- 3 temperature of a cache memory and to develop a signal to
- 4 transition the cache memory from a write-back cache to a
- 5 write-through cache in response to said temperature
- 6 indication.
- 1 36. The circuit of claim 35 wherein said component to
- 2 vary the operation of a system to adjust for the
- 3 temperature affected operation of said cache memory.
- 1 37. The circuit of claim 36 wherein said component to
- 2 adjust a caching operation of the system in response to a
- 3 temperature indication from said memory.

- 1 38. The circuit of claim 36 wherein said component to
- 2 shut off said cache in response to a temperature
- 3 indication.
- 1 39. The circuit of claim 38 wherein said component to
- 2 invalidate a cache line in said cache memory.
- 1 40. The circuit of claim 35 including a cache memory.
- 1 41. The circuit of claim 40 including a ferroelectric
- 2 polymer memory.
- 1 42. The circuit of claim 40 wherein said cache memory
- 2 includes a temperature sensor.
- 1 43. An integrated circuit comprising:
- a ferroelectric polymer memory array; and
- 3 a temperature sensor.
- 1 44. The circuit of claim 43 wherein said array is a
- 2 cache memory.
- 1 45. The circuit of claim 44 wherein said array is a
- 2 disc cache memory.